

Low-power FDDI transimpedance amplifier

SA5222

DESCRIPTION

The NE/SA5222 is a low-power, wide-band, low noise transimpedance amplifier with differential outputs, optimized for signal recovery in FDDI fiber optic receivers. The part is also suited for many other RF and fiber optic applications as a general purpose gain block.

FEATURES

- Extremely low noise: $2.0\text{pA}/\sqrt{\text{Hz}}$
- Single 5V supply
- Low supply current: 9mA
- Large bandwidth: 165MHz
- Differential outputs
- Low output offset
- Low input/output impedances
- High power-supply-rejection ratio: 55dB
- Tight transresistance control
- High input overload: $115\mu\text{A}$
- ESD protected

PIN DESCRIPTION

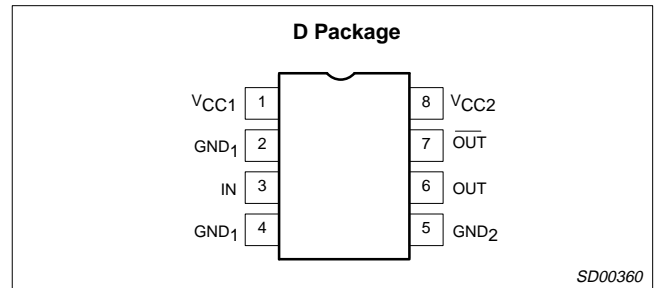


Figure 1. Pin Configuration

APPLICATIONS

- FDDI preamp
- Current-to-voltage converters
- Wide-band gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5222D	SOT96-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC1,2}$	Power supply voltage	6	V
T_A	Ambient temperature range	-40 to +85	°C
T_J	Junction temperature range	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Power dissipation $T_A = 25^\circ\text{C}$ (still air) ¹	0.78	W
I_{INMAX}	Maximum input current	5	mA

NOTE:

1. Maximum power dissipation is determined by the operating ambient temperature and the thermal resistance $\theta_{JA} = 158^\circ\text{C}/\text{W}$. Derate $6.2\text{mW}/^\circ\text{C}$ above 25°C .

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC1,2}$	Power supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range: SA grade	-40 to +85	°C
T_J	Junction temperature range: SA grade	-40 to +105	°C

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DC ELECTRICAL CHARACTERISTICSTypical data and Min and Max limits apply at $T_A = 25^\circ\text{C}$, and $V_{CC1} = V_{CC2} = +5\text{V}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SA5222			UNIT
			Min	Typ	Max	
V_{IN}	Input bias voltage		1.3	1.55	1.8	V
$V_{O\pm}$	Output bias voltage		2.9	3.2	3.5	V
V_{OS}	Output offset voltage			0	± 100	mV
I_{CC}	Supply current		6	9	12	mA
I_{OMAX}	Output sink/source current		1.5	2		mA
I_{IN}	Input current (2% linearity)	Test circuit 5, Procedure 2	± 60	± 90		μA
I_{INMAX}	Maximum input current overload threshold	Test circuit 5, Procedure 4	± 80	± 115		μA
V_{OMAX}	Maximum differential output voltage swing	$R_L = \infty$, Test Circuit 5, Procedure 3		3.6		V_{P-P}

AC ELECTRICAL CHARACTERISTICSTypical data and Min and Max limits apply at $T_A = 25^\circ\text{C}$ and $V_{CC1} = V_{CC2} = +5\text{V}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SA5222			UNIT	
			Min	Typ	Max		
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$, Test Circuit 5, Procedure 1	13.3	16.6	19.9	$\text{k}\Omega$	
R_O	Output resistance (differential output)	DC tested	30	60	90	Ω	
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$	6.65	8.3	9.95	$\text{k}\Omega$	
R_O	Output resistance (single-ended output)	DC tested	15	30	45	Ω	
f_{3dB}	Bandwidth (-3dB) ¹	Test Circuit 1	110	140		MHz	
R_{IN}	Input resistance			150		Ω	
C_{IN}	Input capacitance ²			1		pF	
$\Delta R/\Delta V$	Transresistance power supply sensitivity	$V_{CC1} = V_{CC2} = 5 \pm 0.5\text{V}$		1.0		%/V	
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\text{ MAX}} - T_{A\text{ MIN}}$		0.07		%/°C	
I_{IN}	RMS noise current spectral density (referred to input)	Test Circuit 2, $f = 10\text{MHz}$		2.0		$\text{pA}/\sqrt{\text{Hz}}$	
I_T	Integrated RMS noise current over the bandwidth (referred to input) $C_S = 0\text{pF}$	Test circuit 2, $\Delta f = 50\text{MHz}$		15		nA	
		$\Delta f = 100\text{MHz}$		25			
		$\Delta f = 150\text{MHz}$		36			
		$C_S = 1\text{pF}$	$\Delta f = 50\text{MHz}$		17		
		$\Delta f = 100\text{MHz}$		35			
	$\Delta f = 150\text{MHz}$		55				
PSRR	Power supply rejection ratio	DC Tested, $\Delta V_{CC} = \pm 0.5\text{V}$		-55		dB	
PSRR	Power supply rejection ratio ³	$f = 1.0\text{MHz}$, Test Circuit 3		-34		dB	
I_{INMAX}	Maximum input amplitude for output duty cycle of $50 \pm 5\%$ ⁴	Test circuit 4		± 120		μA	
t_r, t_f	Rise and fall times	10 – 90%		2.2		ns	
t_D	Group delay	$f = 10\text{MHz}$		2.2		ns	

NOTES:

- Bandwidth is tested into 50Ω load. Bandwidth into $1\text{k}\Omega$ load is approximately 165MHz .
- Does not include Miller-multiplied capacitance of input device.
- PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use a RF filter in V_{CC} line.
- Monitored in production via linearity and over load tests.

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TEST CIRCUITS

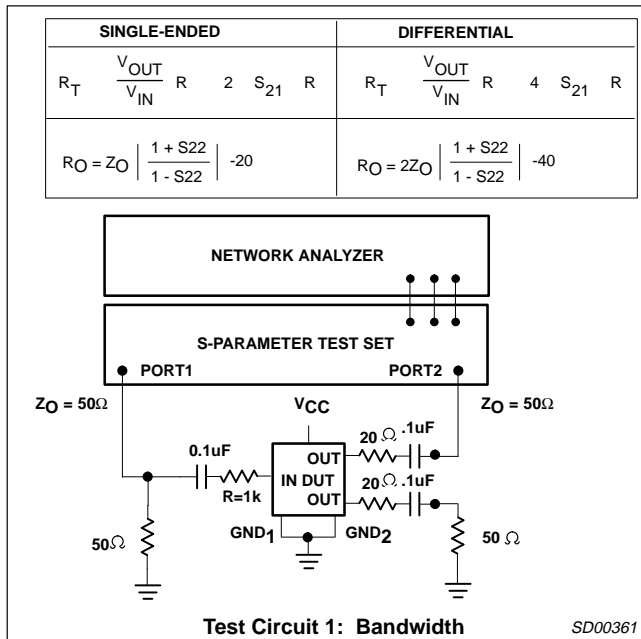


Figure 2. Test Circuit1

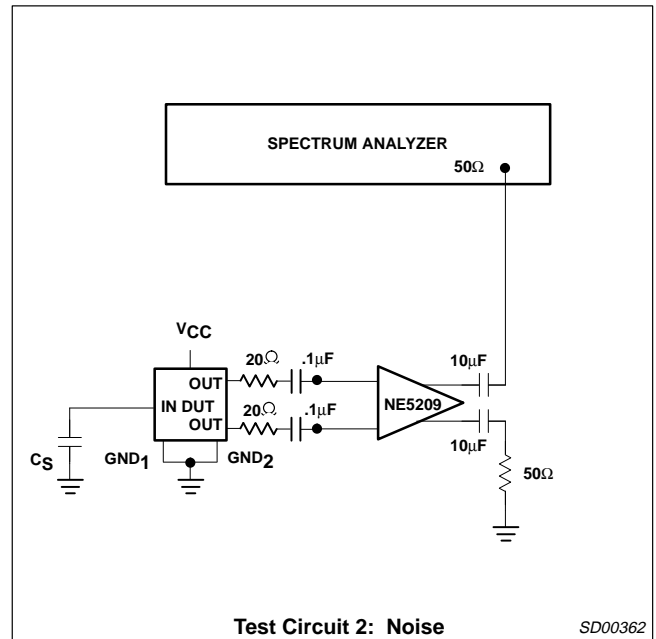


Figure 3. Test Circuit2

TEST CIRCUITS (continued)

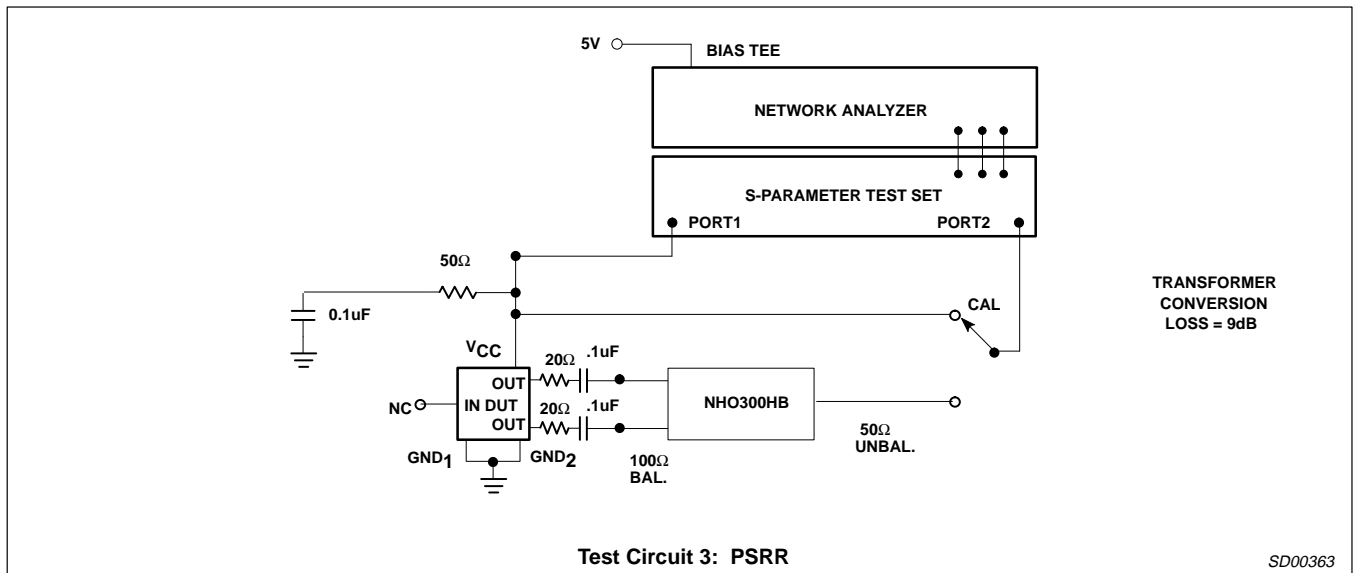


Figure 4. Test Circuit4

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TEST CIRCUITS (continued)

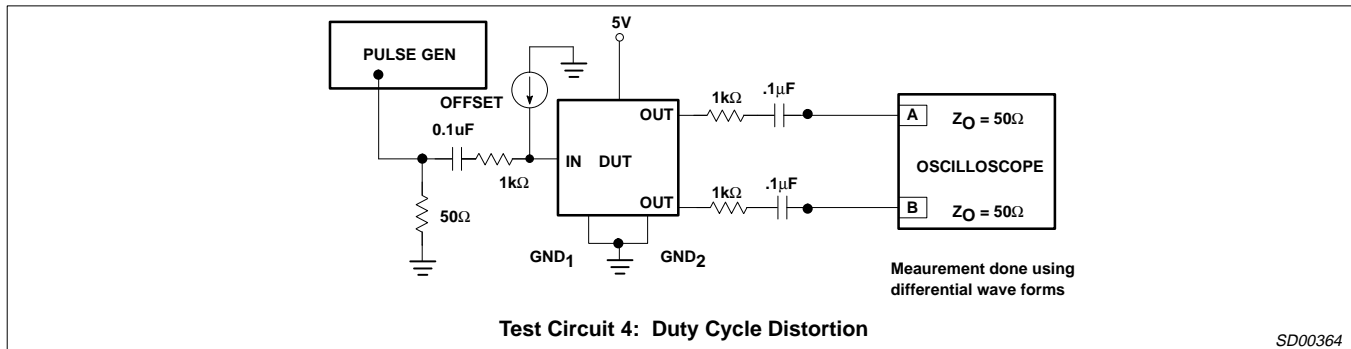


Figure 5. Test Circuit4

TEST CIRCUITS (continued)

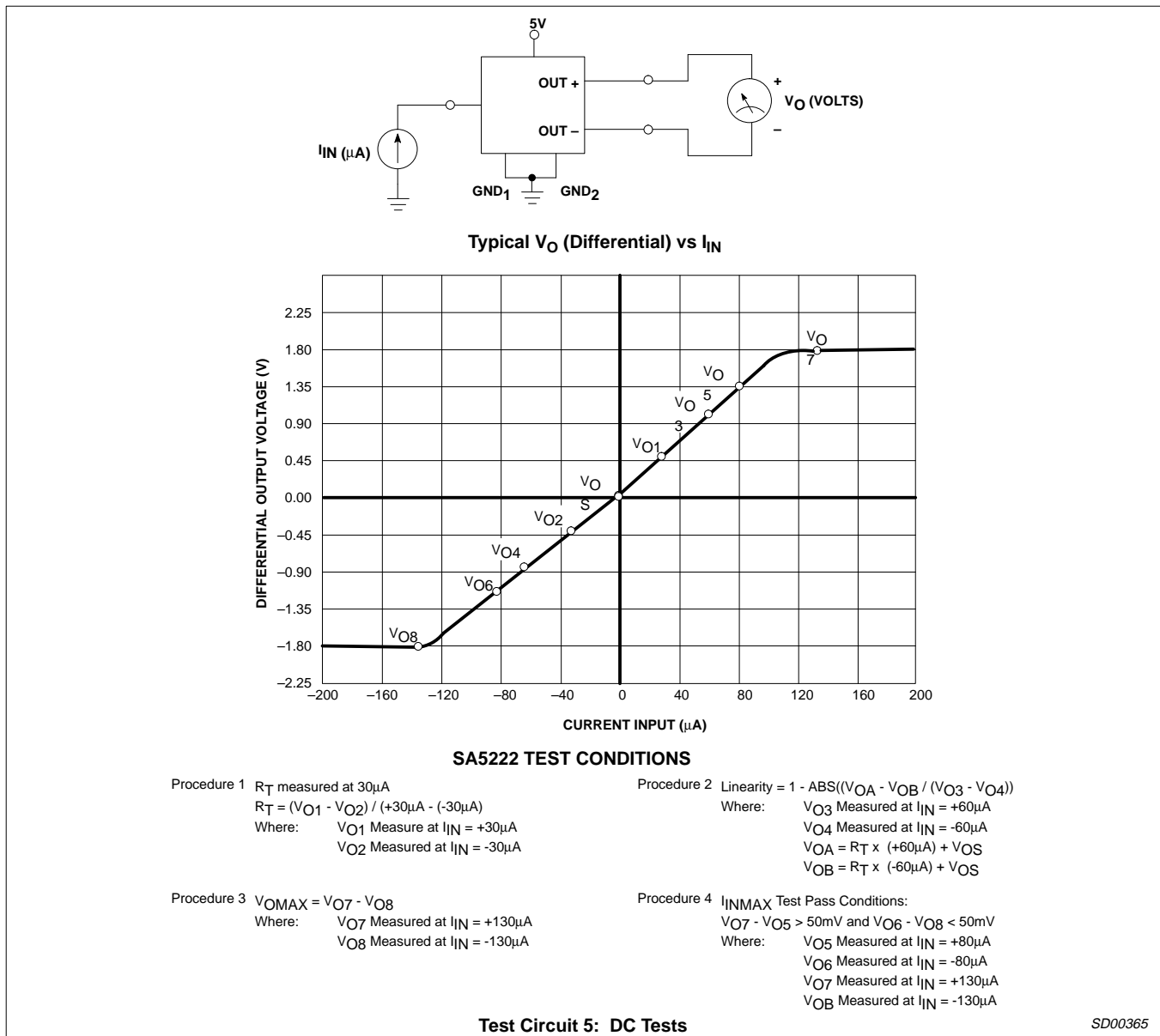


Figure 6. Test Circuit5

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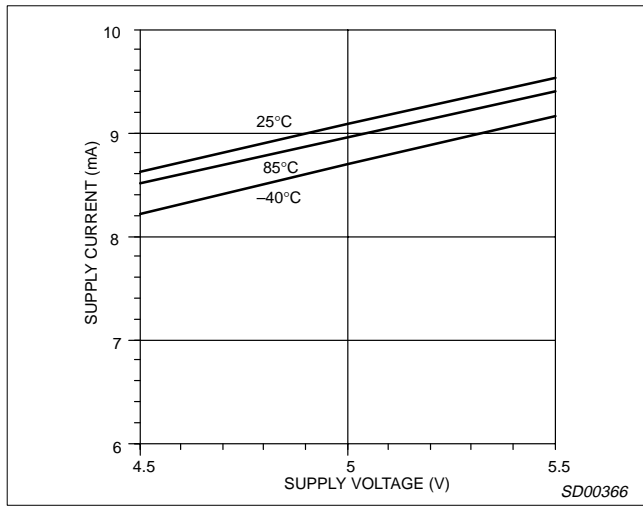


Figure 7. I_{CC} vs. V_{CC} and Temperature

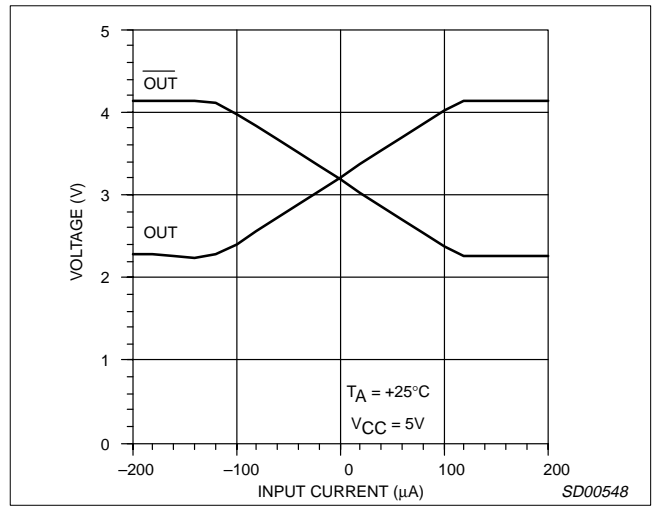


Figure 10. Differential Output Voltages vs. Input Current

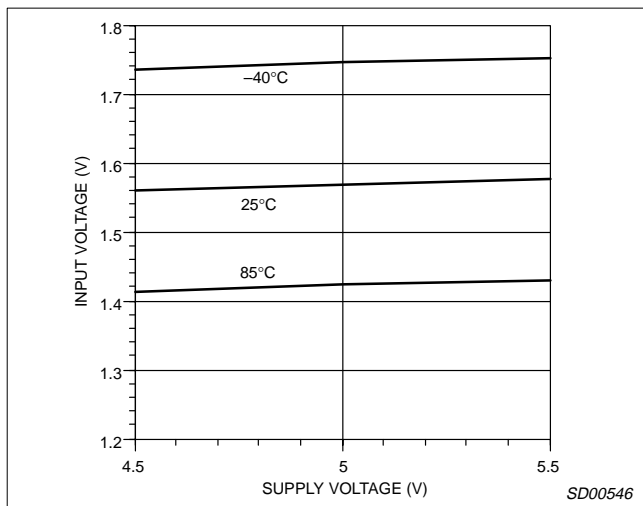


Figure 8. Input Voltage vs. V_{CC} and Temperature

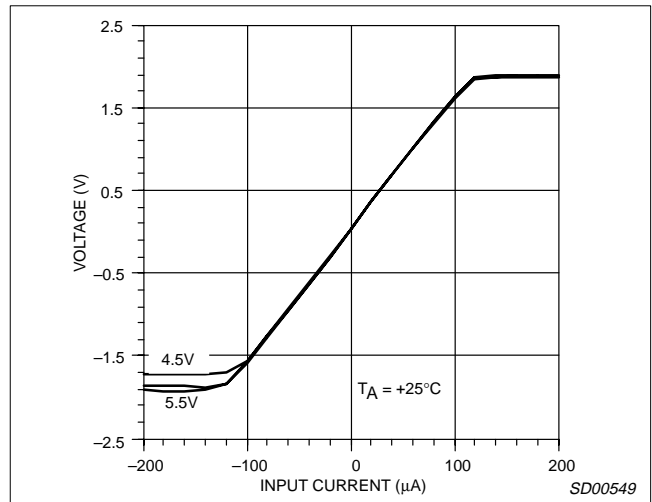


Figure 11. Differential Output Voltage vs Input Current and V_{CC}

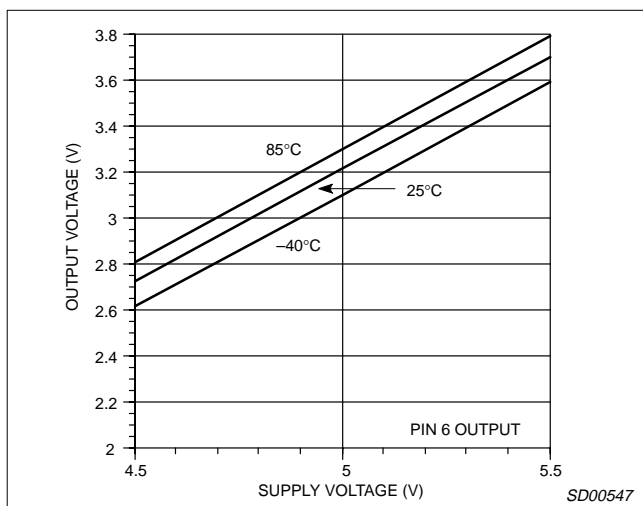


Figure 9. Output Voltage vs. V_{CC} and Temperature

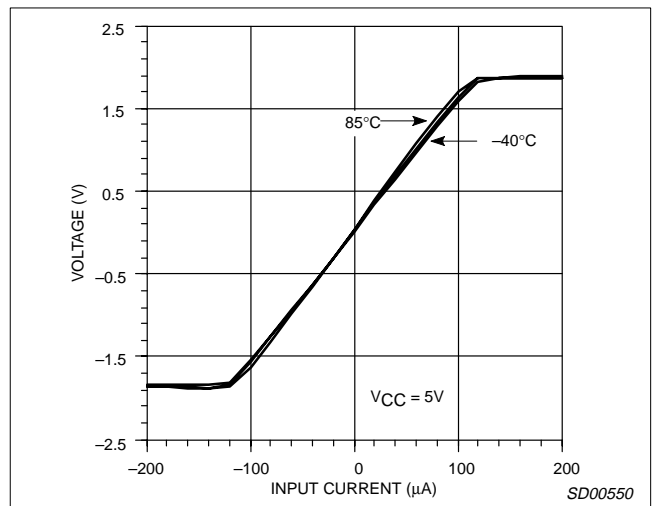


Figure 12. Diff. Output Voltage vs. Input Current and Temp.

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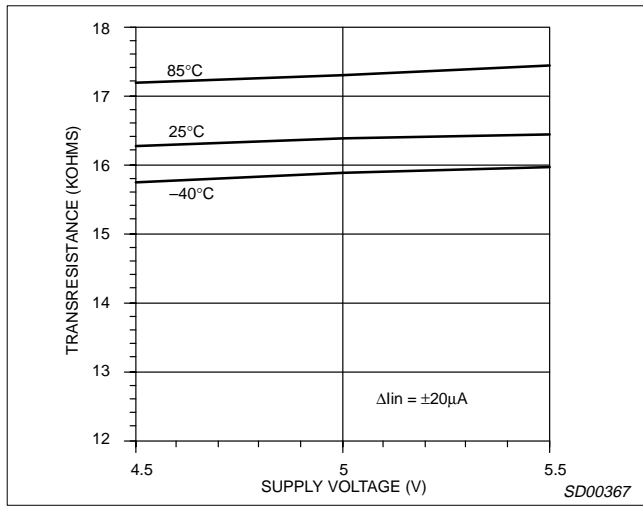


Figure 13. Differential Transresistance vs. V_{CC} and Temperature

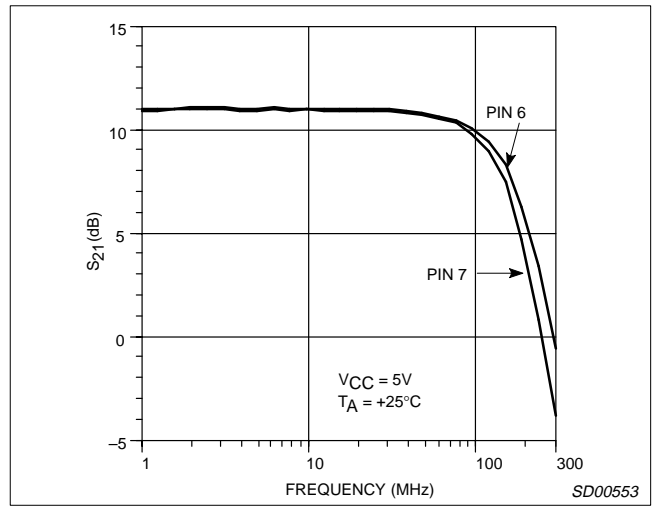


Figure 16. Insertion Gain vs. Frequency

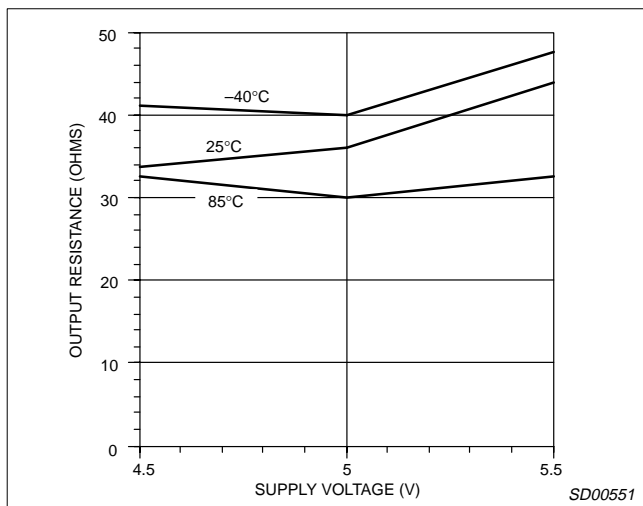


Figure 14. Output Resistance vs. V_{CC} and Temperature

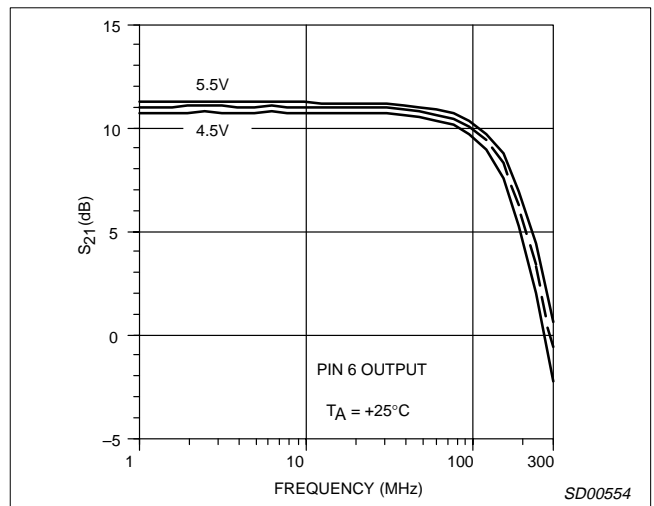


Figure 17. Insertion Gain vs. Frequency and V_{CC}

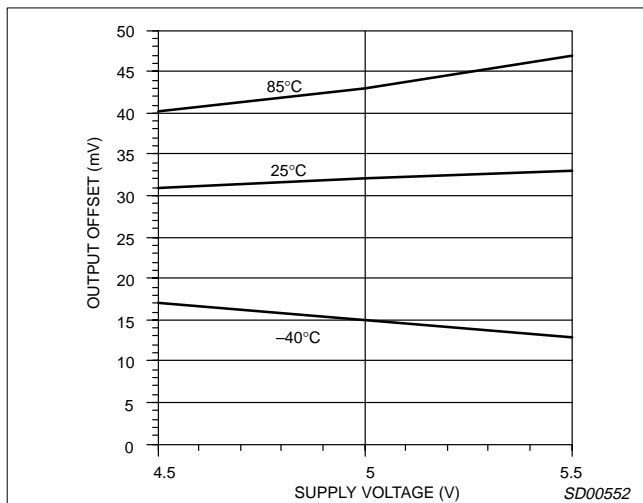


Figure 15. Output Offset Voltage vs. V_{CC} and Temperature

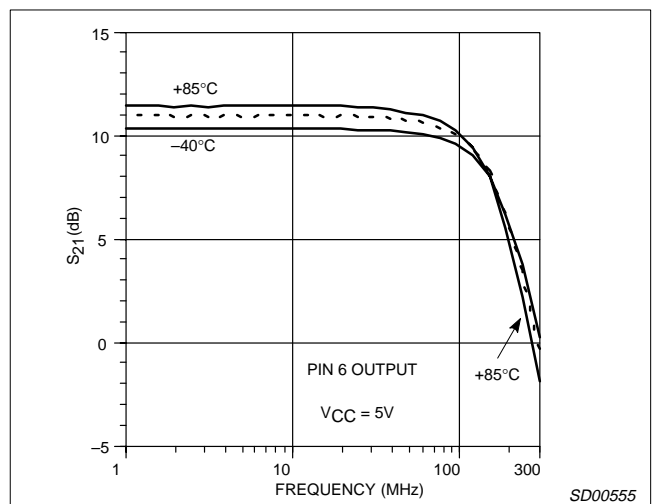


Figure 18. Insertion Gain vs. Frequency and Temperature

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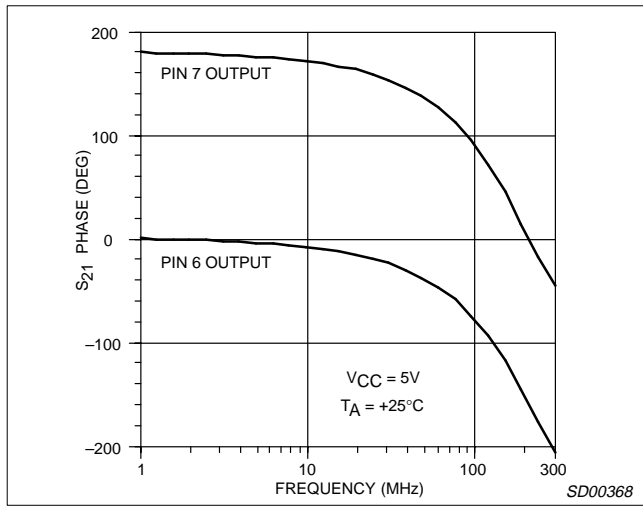


Figure 19. Phase vs. Frequency

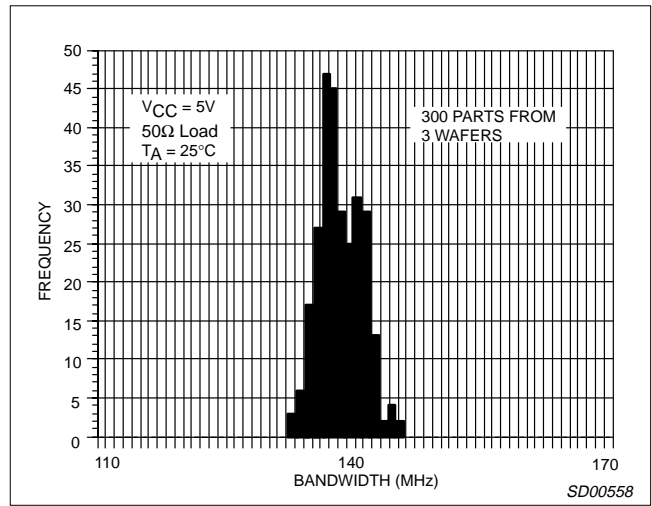


Figure 22. -3dB Bandwidth Distribution

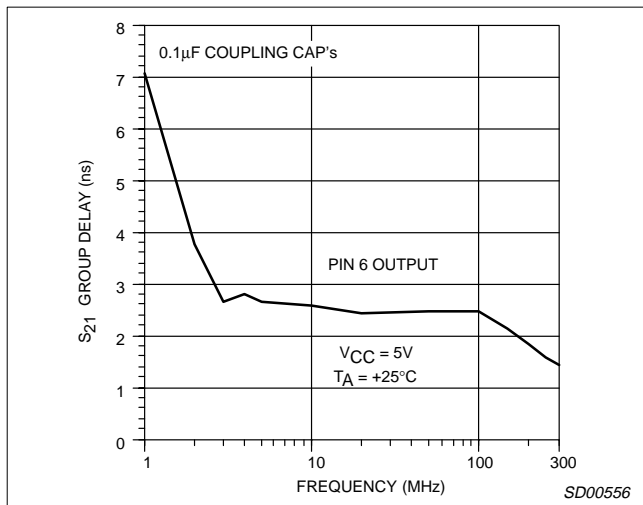


Figure 20. Group Delay vs. Frequency

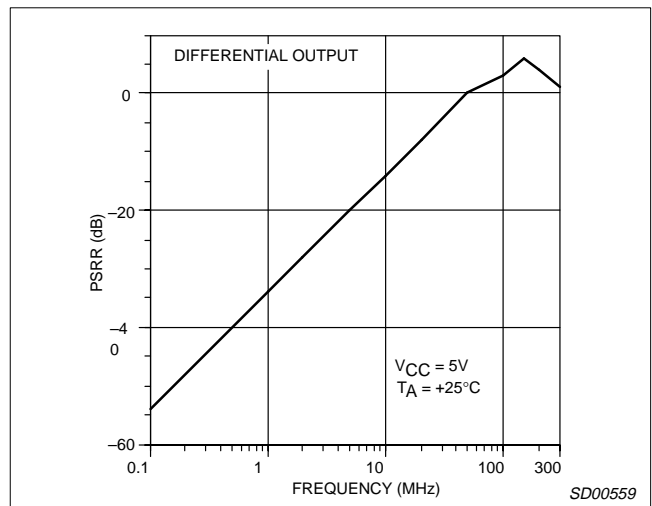


Figure 23. Power-Supply Rejection Ratio vs. Frequency

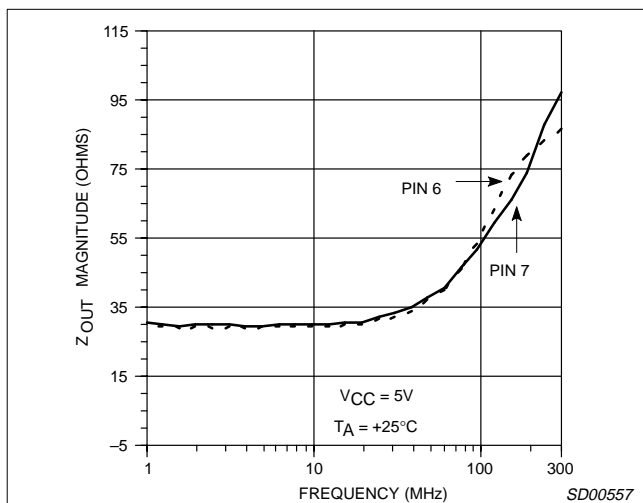


Figure 21. Output Impedance vs. Frequency

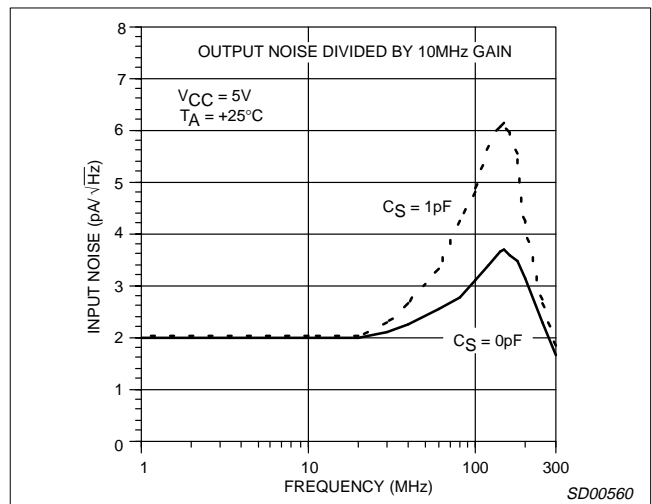
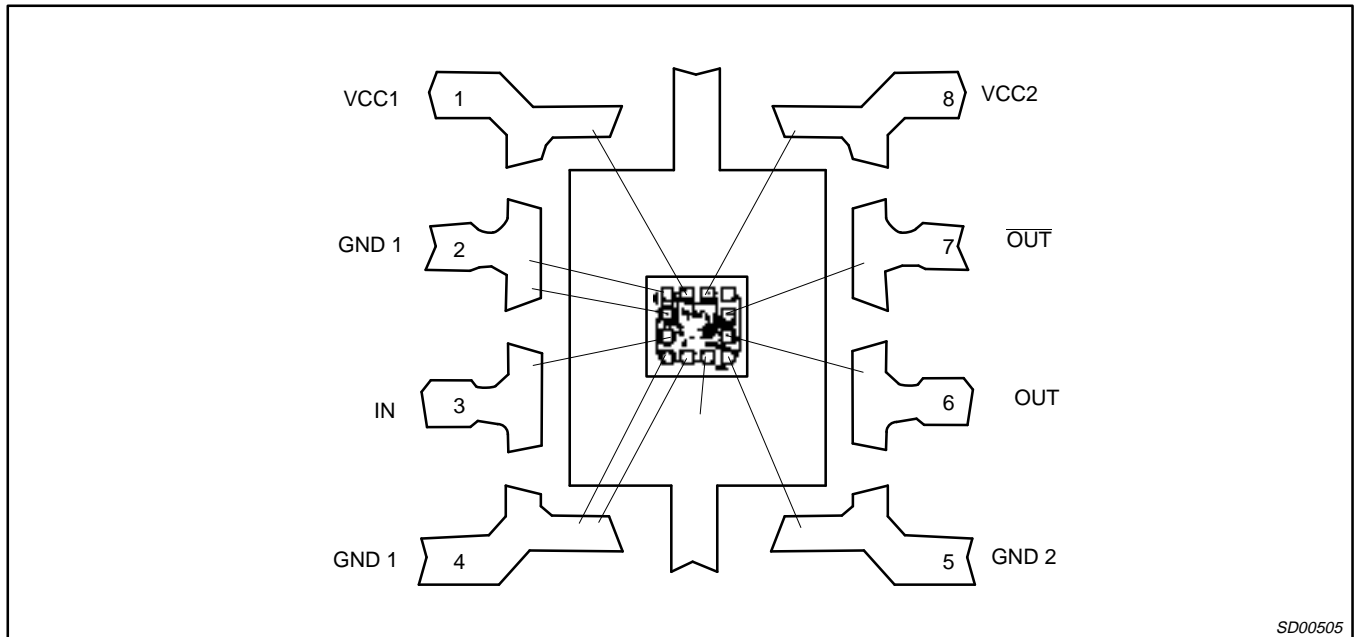


Figure 24. Input Noise Spectral Density vs. Frequency

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SD00505

Figure 25. SA5222 Bonding Diagram

Die Sales Disclaimer

Due to the limitations in testing high frequency and other parameters at the die level, and the fact that die electrical characteristics may shift after packaging, die electrical parameters are not specified and die are not guaranteed to meet electrical characteristics (including temperature range) as noted in this data sheet which is intended only to specify electrical characteristics for a packaged device.

All die are 100% functional with various parametrics tested at the wafer level, at room temperature only (25°C), and are guaranteed to be 100% functional as a result of electrical testing to the point of wafer sawing only. Although the most modern processes are utilized for wafer sawing and die pick and place into waffle pack

carriers, it is impossible to guarantee 100% functionality through this process. There is no post waffle pack testing performed on individual die.

Since Philips Semiconductors has no control of third party procedures in the handling or packaging of die, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems on any die sales.

Although Philips Semiconductors typically realizes a yield of 85% after assembling die into their respective packages, with care customers should achieve a similar yield. However, for the reasons stated above, Philips Semiconductors cannot guarantee this or any other yield on any die sales.